1. A coprocessor interface between a central processing unit (CPU) and a coprocessor, the interface comprising:

an instruction transfer signal group for transferring a plurality of instruction types from the CPU to the coprocessor; and

a busy signal group, coupled to said instruction transfer signal group, for signaling said instruction transfer signal group when one or more of said plurality of instruction types cannot be transferred;

wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types.

2. The coprocessor interface as recited in claim 1 wherein the coprocessor comprises:

A Floating-Point Coprocessor; or

A 3-D Graphics Accelerator.

3. The coprocessor interface as recited in claim 1 wherein said plurality of instruction types comprise:

arithmetic instructions; and

data transfer instructions.

4. The coprocessor interface as recited in claim 3 wherein said data transfer instructions comprise:

TO Coprocessor data transfer instructions; and

FROM Coprocessor data transfer instructions.

5. The coprocessor interface as recited in claim 1 wherein said instruction transfer signal group comprises:

an instruction signal group, for carrying said plurality of instruction types from the CPU to the coprocessor; and

a plurality of strobe signals, each associated with a different one of said plurality of instruction types.

6. The coprocessor interface as recited in claim 5 wherein when one of said plurality of instruction types is dispatched on said instruction signal group, its transfer is completed by assertion of an associated one of said plurality of strobe signals.

7. The coprocessor interface as recited in claim 1 wherein said busy signal group comprises:

an arithmetic busy signal; and

a data transfer busy signal group.

8. The coprocessor interface as recited in claim 7 wherein said data transfer busy signal group comprises:

a TO Coprocessor data transfer busy signal; and

a FROM Coprocessor data transfer busy signal.

9. The coprocessor interface as recited in claim 1 wherein when said busy signal group stops signaling said instruction transfer group that said one or more of said plurality of instruction types cannot be transferred, said instruction transfer group begins transfer of those instruction types, if necessary.

10. The coprocessor interface as recited in claim 1 wherein said instruction transfer signal group transfers two or more of said plurality of instruction types from the CPU to the coprocessor, in parallel.

11. The coprocessor interface as recited in claim 10 further comprising:



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an instruction order signal group, coupled to said instruction transfer signal group, for indicating to the coprocessor a relative execution order for said two or more of said plurality of instruction types that are transferred in parallel.

12. The coprocessor interface as recited in claim 11 wherein said two or more of said plurality of instruction types that are transferred in parallel comprise:

an arithmetic instruction; and

a data transfer instruction.

13. A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a coprocessor interface to be described, said computer readable program code comprising:

first program code for providing an instruction transfer signal group for transferring a plurality of instruction types from a CPU to a coprocessor; and

second program code for providing a busy signal group for signaling said instruction transfer signal group when one or more of said plurality of instruction types cannot be transferred.

14. The computer program product group, as recited in claim 13 wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types.

15. The computer program product group, as recited in claim 14 wherein said instruction transfer signal group comprises:

an instruction signal group, for carrying said plurality of instruction types from the CPU to the coprocessor; and

a plurality of strobe signals, each associated with a different one of said plurality of instruction types.

16. A computer data signal embodied in a transmission medium comprising:

computer-readable first program code for providing an instruction transfer signal group for transferring a plurality of instruction types from a CPU to a coprocessor; and

computer-readable second program code for providing a busy signal group for signaling said instruction transfer signal group when one or more of said plurality of instruction types cannot be transferred;

wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types.

16 ~~17~~. The computer data signal as recited in claim 15 ~~16~~ wherein said instruction transfer signal group transfers two or more of said plurality of instruction types from the CPU to the coprocessor, in parallel.

17 ~~18~~. The computer data signal as recited in claim 16 ~~17~~ further comprising:

computer readable third program code for providing an instruction order signal group, coupled to said instruction transfer signal group, for indicating to the coprocessor a relative execution order for said two or more of said plurality of instruction types that are transferred in parallel.

19. An interface between a central processing unit (CPU) and a coprocessor for transferring data from the CPU to the coprocessor, wherein the data is transferred out-of-order with respect to its associated instructions, the interface comprising:

a data instruction signal group, for transferring first and second data instructions from the CPU to the coprocessor;

a data signal group, coupled to said data instruction signal group, for transferring first and second data, associated with said first and second data instructions, respectively, from the CPU to the coprocessor, out-of-order; and

a data order signal group, coupled to said data group, for indicating to the coprocessor a relative data order of transfer for said first and second data.

20. The interface as recited in claim 19 wherein said first and second data is transferred to the coprocessor without any tag information which would otherwise relate said first and second data with its (their) associated first and second data instructions.

21. The interface as recited in claim 19 wherein said data signal group comprises:

data signals, for dispatching said first and second data from the CPU; and

a TO coprocessor data strobe, coupled to said data signals, for signaling transfer of said first and second data to the coprocessor.

22. The interface as recited in claim 19 wherein said data order signal group comprises:

a data order signal line, for signaling to the coprocessor two distinct relative data orders for said first and second data, at the time said first and second data is transferred.

23. An out-of-order data transfer interface between a central processing unit (CPU) and a coprocessor, comprising:

a data instruction signal group, for transferring M data instructions from the CPU to the coprocessor;

a data signal group, coupled to said data instruction signal group, for transferring M sets of data from the CPU to the coprocessor; and

a data order signal group, coupled to said data signal group, said data order signal group having $2^N$ distinct signals, for indicating to the coprocessor, for each of said M sets of data that are transferred, their relative order of transfer with respect to said M data instructions.

24. The out-of-order data transfer interface as recited in claim 23 wherein said data order signal group comprises three (N=3) distinct signals, for indicating a relative order of transfer for up to 8 outstanding ones of said M sets of data.

25. The out-of-order data transfer interface as recited in claim 23 further comprising:

an order limit signal group, coupled to said data signal group, for signaling a relative data order limit of the coprocessor to the CPU;

wherein when the CPU receives signaling from said order limit signal group, said data signal group, will not exceed said relative data order limit when transferring said M sets of data.

26. The out-of-order data transfer interface as recited in claim 23 wherein said data instruction signal group also transfers M data instructions from the coprocessor to the CPU, said data signal group also transfers M sets of data from the coprocessor to the CPU; and said data order signal group also indicates to the CPU, the relative order of transfer of said M sets of data from the coprocessor with respect to their said M data instructions.

27. A coprocessor interface for establishing instruction, data, and control communication between a central processing unit (CPU) and a coprocessor, the interface providing for coprocessor evaluation of CPU conditional instructions, the interface comprising:

an instruction transfer group for providing the CPU conditional instructions to the coprocessor; and

a condition code check signal group, coupled to said instruction transfer group, for transferring condition code checkss from the coprocessor to the CPU upon evaluation of the CPU conditional instructions by the coprocessor.

28. The coprocessor interface as recited in claim 27 wherein the CPU, upon receipt of said condition code checks from the coprocessor, either executes, or does not execute, the CPU conditional instructions, based on the value of said condition code checks.

29. The coprocessor interface as recited in claim 27 wherein said condition code checks signal the CPU to either execute, or not execute, the CPU conditional instructions.

30. A method for transferring instructions, and data associated with the instructions, from a central processing unit (CPU) to a coprocessor, where the data associated with the instructions is transferred in variable time slots after transfer of their associated instructions, and out-of-order with respect to their associated instructions, the method comprising:

transferring the instructions to the coprocessor;

tracking the number of outstanding instructions that require data for execution; and

providing, along with each data transfer, a relative order indication, to associate each data transfer with one of the number of outstanding instructions that require data for execution;

wherein the coprocessor utilizes the relative order indication to place each data transfer with its associated instruction.

31. The method as recited in claim 30 wherein the coprocessor monitors outstanding instructions that require data for execution from oldest to youngest, and updates the relative order of outstanding instructions upon receipt of each data transfer.